



# UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE  
United States Patent and Trademark Office  
Address: COMMISSIONER FOR PATENTS  
P.O. Box 1450  
Alexandria, Virginia 22313-1450  
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/930,804	08/15/2001	Chris Haywood	06979.0012	3546
33356	7590	05/03/2005	EXAMINER	
SoCAL IP LAW GROUP LLP 310 N. WESTLAKE BLVD. STE 120 WESTLAKE VILLAGE, CA 91362			NGUYEN, TOAN D	
			ART UNIT	PAPER NUMBER
			2665	

DATE MAILED: 05/03/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

# Office Action Summary

Application No.

09/930,804

Applicant(s)

HAYWOOD, CHRIS

Examiner

Toan D Nguyen

Art Unit

2665

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

## Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

## Status

- 1) ☒ Responsive to communication(s) filed on 04 February 2005.
- 2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

## Disposition of Claims

- 4) ☒ Claim(s) 1-4 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 1-4 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_\_ is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

## Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 15 August 2004 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

## Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some \* c) ☐ None of:
- ☐ Certified copies of the priority documents have been received.
  - ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
  - ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

## Attachment(s)

- |  |   |
|--|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892)  | 4) <input type="checkbox"/> Interview Summary (PTO-413)<br>Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948)                                   | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152)             |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)<br>Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____  |

**DETAILED ACTION**

***Claim Rejections - 35 USC § 103***

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

2. Claims 1-4 are rejected under 35 U.S.C. 103(a) as being unpatentable over Bass et al (US 6,557,053) in view of Runaldue et al. (US 6,067,408).

For claim 1, Bass et al. disclose queue manager for a buffer comprising:

a head FIFO memory (figure 1, reference 32) for sequentially delivering data packets (col. 2 lines 10-12);

a tail FIFO memory (figure 1, reference 14) for storing an overflow of said data packets from said head memory and for receiving incoming data packets (col. 1 lines 14-15 and col. 2 lines 24-26);

both said head FIFO memory (figure 1, reference 32) and said tail FIFO memory (figure 1, reference 14) operating at a relatively high data rate equivalent to the rate of the incoming data packets (col. 2 lines 14-21);

a large capacity buffer memory (figure 1, reference 22) having an effectively lower clock rate than said head FIFO memory (figure 1, reference 32) and said tail FIFO memory (figure 1, reference 14) (larger bus width thus has a lower clock rate; col. 3 lines 2-11 and col. 4 lines 7-10), the large capacity buffer memory (figure 1, reference

22) for temporarily storing data overflow from said tail FIFO memory (figure 1, reference 14) (col. 2 lines 24-41);

said head FIFO memory (figure 1, reference 32) and said tail FIFO memory (figure 1, reference 14) in combination with said buffer memory forming the variable size FIFO memory (figure 1, reference 10) (col. 1 line 67 to col. 2 line 12).

However, Bass et al. do not expressly disclose delivering data packets at a relatively slow rate to a plurality of switching elements whereby some latency occurs between said data packets. In an analogous art, Runaldue et al. disclose delivering data packets at a relatively slow rate to a plurality of switching elements whereby some latency occurs between said data packets (figure 1, col. 1 lines 60-65 and col. 4 lines 9-11).

One skilled in the art would have recognized delivering data packets at a relatively slow rate to a plurality of switching elements whereby some latency occurs between said data packets, and would have applied Runaldue et al.'s buffer management system for use in interfacing between asynchronous components, such as local area network and a storage device with variable latency in Bass et al.'s management of queues of data being received from an outside source and inputted into a device for further processing. Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention, to use Runaldue et al.'s full duplex buffer management and apparatus in Bass et al.'s queue manager for a buffer with the motivation being to provide a more efficient buffer memory management system (col. 2 lines 50-53).

For claim 2, Bass et al. disclose wherein said head and tail FIFO memories each have data blocks of a predetermined and same size and wherein said large capacity buffer memory has the same size data block as said head and tail FIFO memories to achieve high efficiency data transfer between said head FIFO memory, said tail FIFO memory and said large capacity buffer memory (col. 4 lines 7-9).

For claim 3, Bass et al. disclose wherein said head and tail FIFO memories reside on a common semiconductor substrate, and wherein said large capacity buffer memory is remote to the semiconductor substrate (figure 1, reference 10, col. 1 lines 46-49 and col. 1 line 66 to col. 2 line 12).

For claim 4, Bass et al. disclose wherein said large capacity buffer memory has a wider bus than a bus included in each of said head and tail FIFO memories (col. 3 lines 2-11).

### ***Response to Arguments***

3. Applicant's arguments with respect to claims 1-4 have been considered but are moot in view of the new ground(s) of rejection.

### ***Conclusion***

4. Applicant's amendment on February 04, 2005 necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire **THREE MONTHS** from the mailing date of this action. In the event a first reply is filed within

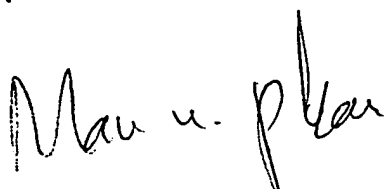
TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

5. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Toan D Nguyen whose telephone number is 571-272-3153. The examiner can normally be reached on M-F (7:00AM-4:30PM).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mr. Huy Vu can be reached on 571-272-3155. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

TN  
TN



MAN U. PHAN  
PRIMARY EXAMINER